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DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP			BELL, PAUL A	
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WASHINGTON, DC 20037-1526			PAPER NUMBER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/876,119

Applicant(s)

KOMURA ET AL.

Examiner

PAUL A BELL

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 March 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 4-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 4-6 and 12-18 is/are rejected.
- 7) ☒ Claim(s) 7-11 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The examiner has some questions regarding the following claim. As pertaining to claim 5, the value of "n" in "a selection period of n times" should be better defined. You must give an example of possible values or range of values for "n". For example does n = the number of sub frames or does it equal the length of time and if that is the case what are the units or is it something else???? When you use "N" lines or "N" rows it is clear it is a whole number representing the number of lines or rows. Also does the "N" lines always equal the "N" rows if this is not the case then you must use a different notation. It is not clear the mathematical relationship of "n times which are fewer in number then N" when it is not clear what "n" can be.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reddy, US 6,175,355 B1 in view of Suzuki, US 5,801,841.

As pertaining to claim 4, Reddy discloses a display panel with a plurality of pixels arranged in rows and columns. In order to display images, a display framed in formed when each pixel in the display is appropriately modulated according to an image. The displayed image is continually updated by displaying a next display frame in a sequence of display frames. Modulating is accomplished by dividing the display panel into blocks of pixels. Each pixel block preferably includes sixteen pixels arranged in a four-by-four array. The gray scale sequences for pixels in a block are offset from one another by various numbers of sub frames. This offset is termed pixel dispersion. The amount of pixel dispersion is preferably not related to an order in which the pixels are arranged in rows and columns within the blocks (col. 2, lines 6-19, 50-67; col. 3, lines 1-37; figs 1-3).

As pertaining to claims 4, Reddy does not directly disclose, "during a predetermined period of time, pixels of a first pixel block of the divided pixel blocks are allocated one of the n gradations and are given one signal and pixels of a second pixel block, adjacent to the first pixel block, of the divided pixel blocks, of the divided pixel blocks are allocated another of the n gradations and are given another signal. "

However since the Reddy device is "used" to produce images on a display, which would require the ability to have different gradations in adjacent pixel blocks to form images therefore this feature is viewed as merely directed towards an "OBVIOUS INTENDED USE" of the Reddy apparatus.

As pertaining to claims 4, Reddy does not disclose "allocating the gradation of n values which are less than the number of $N \times N'$ to each of the pixels of pixel block formed from $N \times N'$ pixels". Reddy instead teaches each PWM grayscale sequence corresponds to a grayscale level for the pixel wherein each of the sub-frames, the pixel is configured in an 'on' condition or in an "off" condition according to selected one of a plurality of predetermined grayscale sequences. Also note gray scaling can be construed as gradation. And further note the Reddy apparatus is capable of being "used" as this limitation suggest where "the gradation of n values are less than the $N \times N'$ ", pixels but this restrictive use of the capable Reddy apparatus is not directly mentioned in text or figures.

As pertaining to claim 4, Suzuki discloses an invention regarding an image signal coding apparatus. In which block truncation coding of an image is divided into pixel blocks (rectangular regions of pixels) and pixels values of a block are approximated by a plurality of representative gradation value and resolution information indicating by which representative value of each pixel is expressed (col. 2, lines 4-8). Figures 13(a) and 13(b) shows an example of coded data and decoded pixel block of the block truncation coding. In the following, it is assumed that the pixel block size is 8 pixels by 8 pixels. An image is reproduced by replacing positions of pixels having resolution information 0 with the representative gradation value A of group 1 and positions of pixels having resolution information 1 with the representative gradation value B of group 0. The two representative gradation values are assigned 16 bits and the resolution information is assigned 64 bits; that is, one pixel block is coded by use of 80 bits (col. 8,

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lines 5-25). Also, figures 14-15 represent another example of the second embodiment. Referring to a block diagram of FIG. 14, a configuration of a coding apparatus according to a second embodiment of the invention will be described. The components in FIG. 14 that are the same as or similar to those in FIG. 2 are given the same reference numerals and descriptions therefor will be omitted. In FIG. 14, a sub-block dividing section 34 divides a pixel block of $m \times n$ pixels (m, n : positive integers) that has been extracted from an image signal by the block extracting section 10 into sub-blocks of $p \times q$ pixels (p, q : positive integers smaller than m and n , respectively). The operation of the coding apparatus of the second embodiment will be described with reference to FIGS. 15(a) and 15(b). FIG. 15(a) shows an example in which a block of 8×8 pixels is divided into sub-blocks of 4×4 pixels. The block truncation coding section 30 performs, for instance, binary block truncation coding on each sub-block. FIG. 15(b) shows an example of coded data produced by binary block truncation coding that is performed on a sub-block basis. For each sub-block, coded data consists of two representative gradation values (2×8 bits) and resolution information ($4 \times 4 = 16$ bits) for 16 pixels. Therefore, the code amount per pixel block is $4 \times (16 + 16) = 128$ bits (col. 9, lines 28-59). So Suzuki disclose to what is said above that allocating the gradation of n values which are less than the number of $N \times N'$ to each of the pixels of pixel block formed from $N \times N'$ pixels.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the gradation technique of Suzuki with the gray scale technique and display of Reddy.

The suggestion/motivation for doing so would have been to provide for a better display that allows for higher resolution, higher definition by using a more reliable gray scale and/or gradation technique.

As pertaining to claim 5 most of the limitations were addressed above in claim 4, in addition the combination of Reddy of Suzuki discloses, "providing signals to the pixels of N lines in a selection period of n times which are fewer number than N", because if interpreted broadly n is equal the number of sub frames and figure 13 of Suzuki illustrates 8 lines with two representative gradation values you would only need two sub frames to a frame to produce gradation therefore $n = 2 < N = 9$.

5. Claims 6, 13, and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reddy in view of Suzuki and further in view of Akiyama et al (hereinafter "Akiyama"), US 5,977,940.

As pertaining to claim 6, Reddy discloses a display panel with a plurality of pixels or pixel electrodes arranged in rows and columns in the form of a matrix. In order to display images, a display framed in formed when each pixel in the display is appropriately modulated according to an image. The displayed image is continually updated by displaying a next display frame in a sequence of display frames. Modulating is accomplished by dividing the display panel into blocks of pixels. Each pixel block preferably includes sixteen pixels arranged in a four-by-four array. The gray scale sequences for pixels in a block are offset from one another by various numbers of sub-frames. This offset is termed pixel dispersion. The amount of pixel dispersion is

preferably not related to an order in which the pixels are arranged in rows and columns within the blocks (col. 2, lines 6-19, 50-67; col. 3, lines 1-37; figs 1-3).

As pertaining to claim 6, it would be obvious that Reddy display would have the following but he does not disclose an X driver for supplying and X signal; an Y driver for supplying and Y signal; a liquid crystal drive voltage supplying circuit for supplying an LC drive voltage to LC drive line arranged in a column direction; an XY calculating circuit for calculating the X and Y signals; a signal comparator for comparing the output of the XY calculating circuit with a reference voltage and outputting a first voltage when the output of the XY calculating circuit is higher than the reference voltage and a second voltage when the lower than that; a switch for controlling the connection of the pixel electrode to the LC voltage line based on the output of the signal comparator; n-gradation approximation calculating circuit and converting the gradation level of each pixel of each block into n-gradation approximation picture signal approximated to n values less than $N \times N'$ and a signal control circuit for controlling all of the above.

As pertaining to claim 6, Suzuki discloses an n-gradation calculating circuit and converting the gradation level of each pixel of each block into n-gradation approximation picture signal approximated to n values less than $N \times N'$ (col. 2, lines 4-8; col. 8, lines 5-25; col. 9, lines 28-59; fig. 2 and 14).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the n-gradation circuit of Suzuki with the gray scale circuit of Reddy.

The suggestion/motivation for doing so would have been to provide for a better display that allows for higher resolution, higher definition by using a more reliable gray scale and/or gradation technique.

As pertaining to claim 6, Akiyama discloses as figure 9 depicts X driver or gate driver 903 for producing a gate signal or X signal; an Y driver or signal driver or producing a Y signal; timing generating circuit 906 for controlling all of the above. As figure 1A depicts a two transistors 8 and 12 and a storage capacitor 2, which can be construed as XY calculating circuit because they take the X and Y signals, calculates another signal representing them and outputs it to a comparator circuit 15 in which a reference voltage is used to compare it to the calculated output signal from the calculating circuit (col. 9, Line 25-col. 10, line 65). Figure 8 depicts an LC driving circuit 204 and Figure 11 C-11 D depicts switches 52. It would be obvious that Akiyama has many different embodiments in which a different design could be implemented that included all the components in one display.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the LCD of Akiyama with that of Reddy and Suzuki.

The suggestion/motivation for doing so would have been to provide a display that included all of the components in one display, even though it would be obvious that all TFT-LCD would have all of the components above even though it might not be shown. But by combining Akiyama with Reddy and Suzuki the display is able to produce higher resolution and higher definition displays.

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As pertaining to claim 13, Reddy discloses a plurality of row lines and column lines, in which a pixel electrode is provided at the intersection of the row and column lines (col. 2, lines 6-19, 50-67; col. 3, lines 1-37; figs 1-3). Akiyama discloses the same thing but also provides the Y signal, the X signal, pixel electrodes and switching elements at the intersection parts of the rows and columns for controlling the connection of a data signal line and pixel electrode according to the calculating value of corresponding signals (col. 9, line 25-col. 10, line 65; fig. 1A). Claim 13 is dependent on claim 6 and is rejected on the same basis and what is stated above.

As pertaining to claims 15-17, Reddy discloses the image is displayed based upon an image therefore it must be obvious that Reddy would have a picture generating unit and a display controller (col. 2, lines 6-19, 50-67; col. 3, lines 1-37; figs 1-3). Furthermore, Reddy discloses using a gray scale technique for allocating n values to each pixel of a pixel block. Suzuki uses a gradation technique (col. 9, line 25-col. 10, line 65; fig. 1A) that can be combined with Reddy. Whether the display apparatus or picture generating unit or the display controller has the means for allocating gradation it is all the same thing because it is adapted for a displaying a picture using sometime of apparatus. Claims 15-17 are dependent on claim 6 and are rejected on the same basis and what is stated above.

6. Claims 12, 14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reddy as applied to claim 6, in view of Suzuki in view of Akiyama and further in view of Robinder, US 5,485,293.

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As pertaining to claim 12, Reddy discloses a display panel with a plurality of pixels or pixel electrodes arranged in rows and columns in the form of a matrix. In order to display images, a display framed in formed when each pixel in the display is appropriately modulated according to an image. The displayed image is continually updated by displaying a next display frame in a sequence of display frames. Modulating is accomplished by dividing the display panel into blocks of pixels. Each pixel block preferably includes sixteen pixels arranged in a four-by-four array. The gray scale sequences for pixels in a block are offset from one another by various numbers of sub-frames. Thin offset is termed pixel dispersion. The amount of pixel dispersion is preferably not related to an order in which the pixels are arranged in rows and columns within the blocks (col. 2, lines 6-19, 50-67; col. 3, lines 1-37; figs 1-3).

As pertaining to claim 12, it would be obvious that Reddy display would have the following but he does not expressly disclose red, green and blue color pixel electrodes; an X driver for supplying and X signal; an Y driver for supplying and Y signal; a liquid crystal drive voltage supplying circuit for supplying an LC drive voltage to LC drive line arranged in a column direction; an XY calculating circuit for calculating the X and Y signals; a signal comparator for comparing the output of the XY calculating circuit with a reference voltage and outputting a first voltage when the output of the XY calculating circuit is higher than the reference voltage and a second voltage when the lower than that; switches for controlling the connection of the colored pixel electrodes to the LC voltage line based on the output of the signal comparator; n-gradation approximation calculating circuit and converting the gradation level of each pixel of each block into n-

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gradation approximation picture signal approximated to n values less than $N \times N'$ and a signal control circuit for controlling all of the above.

As pertaining to claim 12, Suzuki discloses an n -gradation calculating circuit and converting the gradation level of each pixel of each block into n -gradation approximation picture signal approximated to n values less than $N \times N'$ (col. 2, lines 4-8; col. 8, lines 5-25; col. 9, lines 28-59; fig. 2 and 14).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the n -gradation circuit of Suzuki with the gray scale circuit of Reddy.

The suggestion/motivation for doing so would have been to provide for a better display that allows for higher resolution, higher definition by using a more reliable gray scale and/or gradation technique.

As pertaining to claim 12, Akiyama discloses as figure 9 depicts X driver or gate driver 903 for producing a gate signal or X signal; an Y driver or signal driver or producing a Y signal; timing generating circuit 906 for controlling all of the above. As figure 1A depicts a two transistors 8 and 12 and a storage capacitor 2, which can be construed as XY calculating circuit because they take the X and Y signals, calculates another signal representing them and outputs it to a comparator circuit 15 in which a reference voltage is used to compare it to the calculated output signal from the calculating circuit (col. 9, line 25-col. 10, line 65). Figure 8 depicts an LC driving circuit 204 and Figure 11 C-11 D depicts switches 52. It would be obvious that Akiyama has

many different embodiments in which a different design could be implemented that included all the components in one display.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the LCD of Akiyama with that of Reddy and Suzuki.

The suggestion/motivation for doing so would have been to provide a display that included all of the components in one display, even though it would be obvious that all TFT-LCD would have all of the components above even though it might not be shown. But by combining Akiyama with Reddy and Suzuki the display is able to produce higher resolution and higher definition displays.

As pertaining to claim 12, Robinder disclose a liquid crystal display that includes red, green and blue color pixel electrodes and switches with each to the LC drive lines (col. 6, line 19-col. 8, line 1-26; fig. 3).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the color electrodes and switches of Robinder with the LCD of Reddy, Suzuki and Akiyama.

The suggestion/motivation for doing so would have been to provide a display that able to operate as a color display or monochromatic that also can provide higher resolution and higher definition.

As pertaining to claim 14, Reddy discloses a plurality of row lines and column lines, in which a pixel electrode is provided at the intersection of the row and column lines (col. 2, lines 6-19, 50-67; col. 3, lines 1-37; figs 1-3). Akiyama discloses the same thing but also provides the Y signal, the X signal, pixel electrodes and switching

elements at the intersection parts of the rows and columns for controlling the connection of a data signal line and pixel electrode according to the calculating value of corresponding signals (col. 9, line 25-col. 10, line 65; fig. 1A). Furthermore, Robinder discloses red, green and blue color pixel electrodes and corresponding switches (col. 6, line 19-col. 8, line 1-26; fig. 3). Claim 14 is dependent on claim 6 and is rejected on the basis and what is stated above.

As pertaining to claim 18, Reddy discloses a plurality of row lines and column lines, in which a pixel electrode is provided at the intersection of the row and column lines (col. 2, lines 6-19, 50-67; col. 3, lines 1-37; figs 1-3). Akiyama discloses the same thing but also provides the Y signal, the X signal, pixel electrodes and switching elements at the intersection parts of the rows and columns for controlling the connection of a data signal line and pixel electrode according to the calculating value of corresponding signals (col. 9, line 25-col. 10, line 65; fig. 1A). Furthermore, Robinder discloses red, green and blue color pixel electrodes and corresponding switches (col. 6, line 19-col. 8, line 1-26; fig. 3). It would be obvious since Reddy discloses the use of frames and sub-frames that the frame frequency would fall into the range of the limitation.

Allowable Subject Matter

7. Claims 7-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments filed 3/3/04 have been fully considered but they are not persuasive.

The applicant argues on page 13 and 14 with regard to claim 4 that neither Reddy nor Suzuuki teach or suggest, "a pixel matrix is divided into a plurality of pixel blocks, and, during a predetermined period of time, pixels of a first pixel block of the divided pixel blocks are allocated one of the n gradations and are given one signal and pixels of a second pixel block, adjacent to the first pixel block, of the divided pixel blocks, of the divided pixel blocks are allocated another of the n gradations and are given another signal." The examiner disagrees and references rejection above where this newly added limitation is addressed.

The applicant argues on page 14 with regard to claim 5 that neither Reddy nor Suzuuki teach or suggest, "providing signals to the pixels of N lines in a selection period of n time which are fewer in number than N ". The examiner disagrees because of the 112 problems if interpreted broadly n is equal the number of sub frames and figure 13 of Suzuki illustrates 8 lines with two representative gradation values you would only need two sub frames to a frame to produce the two gradation values therefore $n = 2 < N = 9$

The applicant argues on pages 14 and 15 with regard to claims 6 and 12 that neither Reddy, Suzuuki, Akiyama and Robinder teach or suggest, XY calculating circuit, signal comparator and switch. The examiner disagrees and references the rejection above where it was shown how Akiyama et al. reference teaches this in figure 1A.

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In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Bell whose telephone number is (703) 306-3019.


If attempts to reach the examiner by telephone are unsuccessful the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377 can help with any inquiry of a general nature or relating to the status of this application.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Or Faxed to: (703) 872-9306

Or Hand-delivered to: Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor
(Receptionist)


Paul Bell
Art unit 2675
May 17, 2004


CHANH NGUYEN
PRIMARY EXAMINER